What is Claimed is:

[c1] A method for forming a transistor, the method comprising the steps of:

a) providing a semiconductor substrate;

b) patterning the semiconductor substrate to provide a first body edge;

c) providing a gate structure adjacent the first body edge;

d) patterning the semiconductor substrate to provide a second body edge, the first and second body edges of the semiconductor substrate defining a transistor body;

e) providing a body contact structure adjacent the second body edge aligned to the gate structure; and

f) providing an electrically connective bridge between the gate structure and the body contact structure over the transistor body.

[c2] The method of claim 1 wherein the semiconductor substrate comprises a silicon-on-insulator layer, and wherein the step of patterning the semiconductor substrate to provide first body edge comprises patterning the silicon on the silicon-on-insulator layer and wherein the step of patterning the semiconductor substrate to provide a second body edge comprises patterning the silicon layer on the silicon-on-insulator layer.

[c3] The method of claim 1 further comprising the steps of forming a gate dielectric layer on the first body edge.

[c4] The method of claim 1 further comprising the steps of forming a diffusion barrier layer on the second body edge.

[c5] The method of claim 1 further comprising the steps of forming an insulator layer on the top of the fin body and below the bridge.

[c6] The method of claim 1 wherein the step of patterning the semiconductor substrate to provide a first body edge comprises forming a mandrel layer on the semiconductor substrate; patterning the mandrel layer to form an exposed side, and forming a sidewall spacer adjacent to the exposed side, and wherein a first edge of the sidewall spacer defines the first body edge.

[c7] The method of claim 6 wherein the step of patterning the semiconductor substrate to provide a second body edge comprises using a second edge of the sidewall spacer to define the second body edge.

[c8] The method of claim 1 further comprising the step of forming source and drain implants into the body of the transistor by performing an angled implant into the transistor body.

[c9] The method of claim 8 wherein the step of forming a source and drain implants in the transistor body comprises performing a plurality of angled implants into the body.

[c10] The method of claim 1 wherein the step of patterning the semiconductor substrate to provide a first body edge comprises forming a mandrel layer on the semiconductor substrate; patterning the mandrel layer, and using the patterned mandrel layer to define the first body edge.

[c11] The method of claim 10 wherein the step of patterning the semiconductor substrate to provide a second body edge comprises forming a sidewall spacer adjacent to a mandrel layer and using the sidewall spacer to define the second body edge.

[c12] A transistor comprising:

a) a transistor body formed on a substrate, the transistor body having a first vertical edge and a second vertical edge;

b) a gate structure adjacent the transistor body first vertical edge;

c) a body contact structure adjacent the transistor body second vertical edge and aligned with the gate;

d) a bridge over the body, the gate, and the body contact, electrically connecting the gate and the body contact; and

e) source and drain regions in the body on opposite ends of the body.

[c13] The transistor of claim 12 wherein the gate structure comprises p-type material and wherein the body contact structure comprises n-type material.

[c14] The transistor of claim 12 wherein the gate structure comprises n-type material and wherein the body contact structure comprises p-type material.

[c15] The transistor of claim 12 wherein the transistor body comprises a portion of silicon of the silicon-on-insulator layer.

[c16] The transistor of claim 12 wherein the thickness of the transistor body between the gate structure and the body contact structure is less than one-third of the length of the gate structure.

[c17] The transistor of claim 12 further comprising a gate dielectric between the transistor body first edge and the gate structure and a diffusion barrier between the transistor body second edge and the body contact structure.

[c18] The transistor of claim 12 wherein the transistor body comprises source and drain implants into the transistor body, the implants aligned with the edges of the body contact and the gate structure.

[c19] The transistor of claim 12 wherein the body comprises widened end portions that are insulated from the gate and the body contact.

[c20] The transistor of claim 12 wherein the transistor body first edge is opposite the transistor body second edge and wherein the transistor body first edge and transistor body second edge are substantially perpendicular to a top surface of the substrate.

[c21] A dynamic threshold complimentary metal oxide semiconductor field effect transistor comprising:

a) a transistor body, the transistor body formed from a silicon layer formed above an insulator layer, the transistor body having a first vertical edge and a second vertical edge, wherein the transistor body first edge and the transistor body second edge are opposite each other and substantially perpendicular to the insulator layer, thereby defining a fin-type transistor body;

b) a gate dielectric layer formed on the transistor body first edge;

c) a body contact native oxide layer formed on the transistor body second edge;

d) a gate structure formed on the gate dielectric layer adjacent to the transistor body first edge, the gate structure comprising p-type polysilicon; and

e) a body contact structure formed on the body contact native oxide layer aligned to the gate structure and adjacent to the transistor body second edge, the body contact structure comprising n-type polysilicon..

[c22] A dynamic threshold complimentary metal oxide semiconductor field effect transistor of claim 21 wherein the gate structure comprises n-type polysilicon and the body contact structure comprises p-type polysilicon.

[c23] The dynamic threshold complimentary metal oxide semiconductor field effect transistor of claim 21 wherein the body comprises a substantially uniform dopant concentration density

in the source and drain regions.

[c24] The dynamic threshold complimentary metal oxide semiconductor field effect transistor of claim 23 wherein the substantially uniform dopant concentration density is formed by performing a plurality of angled implants into the transistor body.

[c25] The dynamic threshold complimentary metal oxide semiconductor field effect transistor of claim 21 further comprising a metal silicide bridge over the body to electrically couple the gate structure to the body contact structure.